ABSTRACT

In-circuit-emulation of an integrated circuit including a digital data processor capable of executing program instructions. A first debug event is detected during normal program execution. The causes the in-circuit-emulation to suspend program execution except for real time interrupts. A debug frame counter increments on each interrupt and decements on each return from interrupt. If a debug event is detected during an interrupt service routine, that interrupt service routine is suspended and teh count of the debug frame counter is stored. Execution of other interrupt service routines in response to corresponding interrupts is still permitted. The integrated circuit includes plural debug event detectors and the debug frame count is stored at the detector detecting a debug event during an interrput service routine. This permits a determination of the order of interrupts triggering debug events by reading the stored debug frame count from each debug event detector.